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SUPPLEMENTARY INFORMATION

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Revisiting the δ-phase of poly(vinylidene fluoride) for solution-processed ferroelectric thin films

By Mengyuan Li[1]*, Harry J. Wondergem[2], Mark-Jan Spijkman[1], Kamal Asadi[2], Ilias Katsouras[1], Paul W. M. Blom[1,3] *and* Dago M. de Leeuw[1,3]

[1] Zernike Institute for Advanced Materials, University of Groningen, Nijenborgh 4, 9747 AG, Groningen, The Netherlands

[2] Philips Research Laboratories, High Tech Campus 4, 5656 AE, Eindhoven, The Netherlands

[3] Max Planck Institute for Polymer Research, Ackermannweg 10, 55128 Mainz, Germany

[*] E-mail: mengyuan.li@rug.nl

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Table of Contents

1. Supplemental Introduction

The supplemental information contains the experimental details about film preparation, microstructure characterization, dielectric measurements and electrical characterization such as polarization data retention and programming cycle endurance. AFM images of as deposited films are given. Capacitors made with smooth, thinner d-PVDF films are presented. The molecular mobility of δ-PVDF is investigated by dielectric spectroscopy at temperatures between -80 °C and 200 °C. The dielectric constants are given as a function of frequency and temperature. A preliminary interpretation is discussed. Finally, the first field-effect transistors using a ferroelectric PVDF gate dielectric are presented. Both a ferroelectric single channel transistor and a ferroelectric dual-gate transistor are presented.

2. Supplemental Methods

PVDF with molecular weights, M_w, of 180, 275, and 534 kg/Mol was purchased from Sigma-Aldrich. PVDF has a limited solubility in common organic solvents such as alcohols, chlorinated solvents and acids. Good solvents are *e.g.* N,N-dimethylformamide (DMF), dimethylsulfoxide and N-methyl-2-pyrrolidone. Here we used solutions of PVDF in DMF, typically 10% by weight for wire-bar coating and 5% for spin-coating. Thin PVDF films were made in a standard class 10,000 clean room with a temperature of 20 ^{o}C and a relative humidity of 45% by both wire-bar (Meyer rod) coating and spin-coating. The substrate temperature for the wire-bar coater was controlled using a K202 control coater (RK Print) between room temperature and 140 ^{o}C. The substrate used for spin-coating was heated in situ with a heat gun and the temperature was measured with a contactless IR thermometer (RS-components 1327K). After coating, the films were either a) dried, annealed at 150 °C and slowly cooled down to room temperature or b) melted at 200 °C, quenched in ice water and annealed at 150 °C.

The film thickness was measured with a Dektak profilometer. The surface morphology of the films was characterized by atomic force microscopy (AFM) (Nanoscope Dimension 3100 Bruker). To ascertain the crystal phase of the films, both grazing incidence X-ray diffraction (GI-XRD) and Fourier-transform infrared spectroscopy (FTIR) were used. GI-XRD scans were obtained with a Philips X'pert MRD diffractometer, using the line focus of a Cu-anode X-ray tube, a Göbel mirror in the primary beam and a parallel plate collimator in front of the detector. The incidence angle was fixed during the measurement at an angle of 0.23° just above the critical angle of total diffraction. Infrared spectra were recorded using a Bruker Vertex spectrometer attached to a Hyperion FT-IR microscope. The scans were performed with a resolution of 4 cm^{-1}.

Capacitors were fabricated on thermally oxidized silicon monitor wafers on which 50 nm thick Au bottom electrodes on a 2 nm Ti adhesion layer were photo-

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lithographically defined. After film deposition, and/or annealing, the capacitors were finished by evaporating an Au top electrode through a shadow mask. The device area varied from 0.059 to 1.38 mm^2.

To allow phase identification with GI-XRD, large device areas of 1 cm^2 were fabricated without the strongly diffracting Au top electrodes. A thin film of the amorphous conducting polymer PEDOT:PSS, a water-based suspension of poly(3,4-ethylenedioxythiophene) stabilized with poly(4-styrenesulphonic acid), was used instead. As bottom electrodes we used Pd. A PVDF film was applied and the PEDOT:PSS, AGFA ICP 1020 (Agfa-Gevaert) was spin-coated from a formulation containing a few drops of the nonionic Zonyl FSO-100 (DuPont) fluoro-surfactant. The PEDOT:PSS thickness amounted to 100 nm and the conductivity amounted to 300 S/cm. Finally, the redundant PEDOT:PSS was removed by reactive ion etching using a shadow mask.

Electric displacement loops versus electric field for the capacitors were measured using a Sawyer-Tower circuit, consisting of a Tektronix AFG3102 function generator, a Tektronix TDS3032B oscilloscope and a Krohn-Hite 7600 wide-band amplifier. The capacitors were measured with a continuous triangular wave signal, to reduce the time at maximum bias, at a frequency of 100 Hz and using a reference capacitor of 216 nF.

Data retention was measured in a Janis probe station in a dynamic vacuum of 10^{-4} mbar, using a Precision Workstation (Radiant Technologies). A write pulse was applied, followed by two read pulses of the same amplitude but opposite polarity, at fixed intervals ranging between 1 s and 300.000 s. All pulse widths were fixed at 10 ms. The programming cycle endurance was measured using the same setup. A triangular pulse of 160 V_{pp} with a frequency of 200 Hz was applied for spans of time ranging between 1 s and 3000 s. The resulting number of cumulative cycles exceeded 10^6. The remanent polarization after each span was measured with a Positive-UP-Negative-Down (PUND) sequence of 10 ms wide pulses. The molecular mobility of the films was investigated by dielectric spectroscopy at temperatures between –80 °C and 200 °C, using a Schlumberger SI1260 Impedance Gain Phase Analyzer.

3. Microstructure

Thin films were made by wire-bar coating and spin-coating. They behaved qualitatively the same. The crucial parameter is the substrate temperature, as it determines the film roughness. Films deposited at low substrate temperatures exhibit a high roughness. Especially spin-coated films are extremely rough; the rms roughness is comparable to the layer thickness.

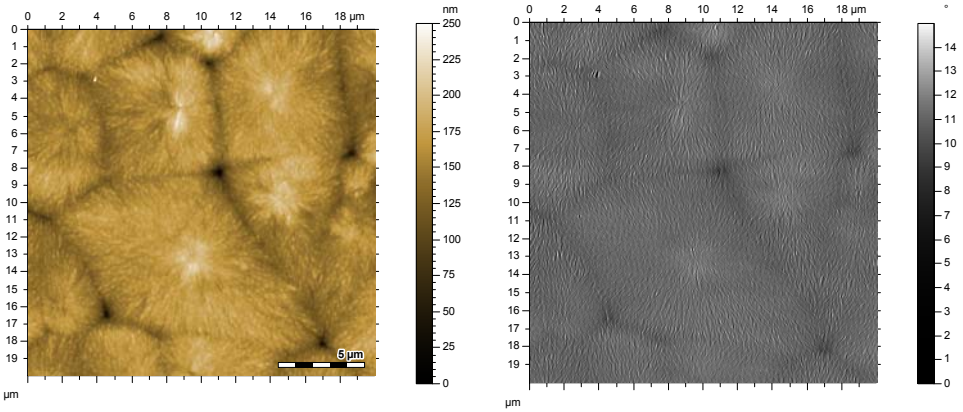

Figure S1. Morphology *(left) height image (right) phase image of a PVDF film spin-coated at 100 ºC.*

Smooth films, however, are obtained at elevated substrate temperatures. Thin films about 400 nm thick, deposited at 100 °C exhibit an rms roughness of less than 10 nm. The roughness is reduced by suppression of the PVDF crystallization through faster evaporation of the solvent, here DMF, and by a smaller driving force, the difference between substrate temperature and crystallization temperature. AFM measurements and optical micrographs showed that the as-cast films contain small spherulites of up to 10 µm, typical for microcrystalline α-PVDF. A height and phase image of a 400 nm thin film spin-coated at 100 ºC is presented in Fig. S1.

4. Thin film capacitors

We have fabricated thinner films by reducing the solid weight content of PVDF in the DMF solution. The films were spincoated at 90 ^{o}C. Fig. S2 shows the film thickness (red symbols left axis) and the rms roughness (black symbols right axis) as a function of PVDF content. The films remain extremely smooth. The roughness for thin films is between 1 and 2 nm.

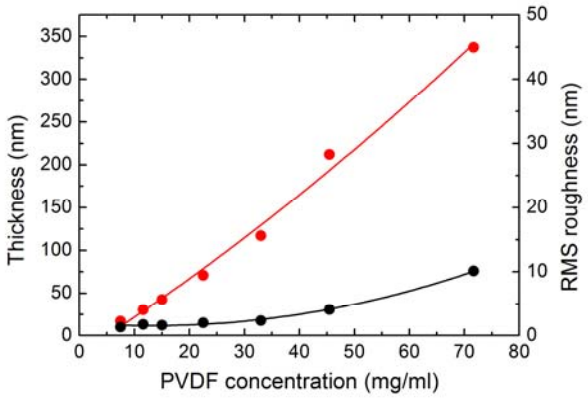

Fig. S2. Topography of PVDF thin films. *Thickness and rms roughness of PVDF thin films as a function of PVDF content in DMF. Films were prepared by spincoating at 90 ^{0}C. Red symbols represent the layer thickness, left axis. Black symbols represent the RMS roughness, right axis.*

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Ferroelectric δ-PVDF films could be fabricated by electro-forming. Fig. S3 shows both the forming voltage and the coercive voltage as a function of layer thickness. A linear relation is found, showing that the forming field and the coercive field are about 120 MV/cm and 250 MV/cm. The data shows that a reduction of the layer thickness leads to a concomitant decrease in coercive voltage. The inset shows the saturated hysteresis loops. The remanent polarization does not depend on layer thickness and amounts to 7 μC/cm^2. The optimization of the process technology to arrive at reliable ferroelectric δ-PVDF thin films below 50 nm is on-going but beyond the scope of this paper.

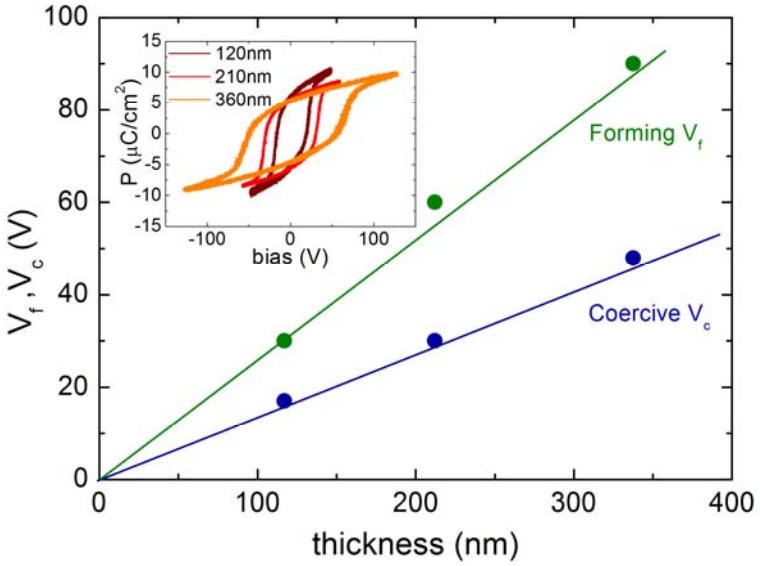

Fig. S3. Scaling of δ-PVDF. *Forming voltage and coercive voltage of δ-PVDF as a function of layer thickness. The linear relation found yields a forming field of 250MV/cm and a coercive field of 120 MV/cm. The inset shows the saturated hysteresis loops for various film thicknesses. The remanent polarization in all capacitors amounted to* 7 μC/cm^2.

We note that the relatively high value of the coercive field of the organic ferroelectrics of about 100 MV/m stems from the large-scale rotation of the individual macromolecules upon polarization reversal.[1] To obtain low-voltage operation of transducers and non-volatile memories thin ferroelectric films are required. Usually thermal annealing above the Curie temperature is required to render the polymer ferroelectric. However, annealing causes grain growth and an increase in surface roughness. Nevertheless, for the copolymer even ultrathin films have been obtained.[2,3] For δ-PVDF thermal annealing is not needed, the phase is formed by electropoling. Fabrication of ultrathin films should be feasible.

5. Alternative chain packing model for α-PVDF

The direction of the polymer chains in α-PVDF is described in this manuscript as alternating left oriented and right oriented, with respect to the slanting direction of the C-F bonds. There is, however, an alternative description;[4,5] the directions of the polymer chains can be fully random. Both models fulfill the symmetry conditions of the α-PVDF space group. The chain directions will be conserved when δ-PVDF is formed; hence the two models for α-PVDF result in two models for δ-PVDF. X-ray diffraction data suggests that both the alternating and random form of α-PVDF exists, with the statistical packing being preferred for material formed during fast cooling from the melt, and the alternating packing being preferred for slowly annealed samples.[6] An elegant alternative explanation for the seemingly statistical packing has been given by Takahashi *at al.*. They concluded that α-PVDF forms an anti-phase domain structure. Within each domain the directions of the chains are alternating.[7] Between two domains a shift exists of half a unit cell in both the a- and b-direction. When these domains are small enough, the diffracted intensities will be influenced enough to suggest the presence of a statistical packing.

6. Molecular mobility of δ-PVDF

The molecular mobility of δ-PVDF has been investigated by dielectric spectroscopy at temperatures between –80 °C and 200 °C, from below the glass transition temperature to above the melting point. The complex dielectric constant is presented as a function of frequency, from 30 Hz to 300 kHz, and temperature in Fig. S4. Two relaxations are observed. The broad relaxation around –20 °C shifts with increasing frequency to higher temperature. In analogy to neat paraelectric α-PVDF, this relaxation is assigned to the α_a relaxation, which is due to segmental motions in the amorphous phase.[8] Similarly, the broad relaxation at around 100 °C is assigned to the α_c relaxation arising from dipolar relaxations of imperfections in the crystalline parts of the film. This relaxation is absent in amorphous PVDF. The dielectric loss at the onset of melting linearly increases with reciprocal frequency. The origin of this so-called Warburg impedance is ionic conductivity.

These dielectric losses could be suppressed by applying a small fixed DC bias. The finite dielectric loss at very low temperature might be stemming from a weak and broad β-relaxation due to motions in the glassy state. The α_a relaxation for δ-phase PVDF is comparable to that of the independently measured α-phase PVDF. The microscopic dynamics of the α_c relaxation, however, appears to be different. The shift in temperature of the maximum dielectric constant with increasing frequency for α-phase PVDF could be described with the Vogel-Fulcher equation,[9] while the temperature of maximum dielectric constant for δ-phase PVDF hardly shifts with frequency. The difference might be attributed to different imperfections in the crystalline parts, as the α_c relaxation is due to motions of disordered chain fragments between crystal lamellae,[10] but the microscopic origin has not been identified.

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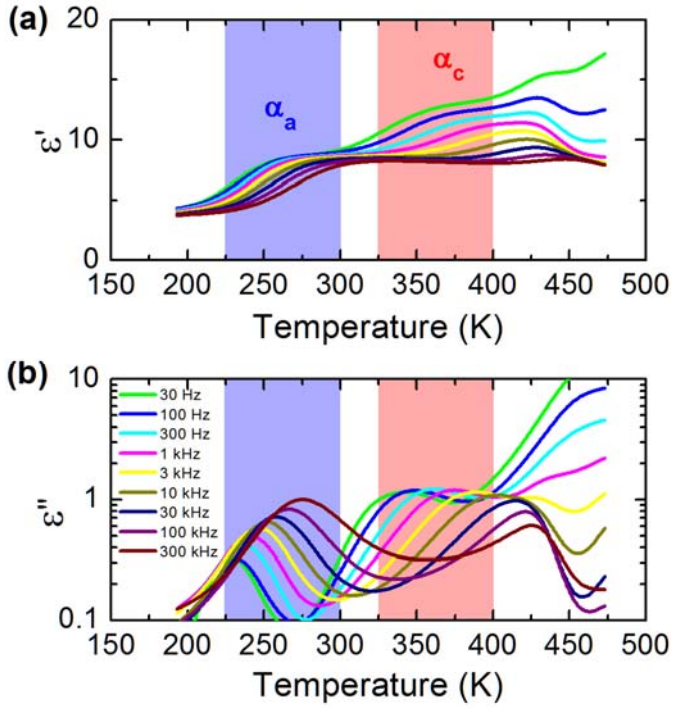

***Figure S4. Molecular mobility**. Real, ε', and imaginary, ε", parts of the dielectric constant of δ-phase PVDF as a function of temperature between 180 K and 470 K and of frequency from 30 Hz to 300 kHz. The α_a relaxation at around 250 K is due to segmental motions in the amorphous phase and the broad α_c relaxation at around 350 K is due to dipolar relaxations by imperfections in the crystalline parts.*

7. Field-effect transistors

Organic ferroelectrics can be used in a wide range of applications such as touch control, piezo and pyroelectric detectors, transducers, non-volatile memories and energy harvesting. For instance poled polymers for sensors and photonic applications such as thermal and ultrasonic imaging have been reviewed already in 1996.[11] The progress in piezoelectric polymers until 2000 has been reviewed by Fukada et al.[12] and on patterned piezo, pyro and ferroelectricity of poled polymers up to 2010 by Qiu.[13] Integrated infrared sensors,[14] an all-printed ferroelectric active matrix sensor network,[15] a sheet type communication system[16] and a Braille display where P(VDF-TrFE) is used as a transducer have been reported.[17] Applications are envisaged in conformable touch keypads, electronic skin and panoramic motion sensors.

A major commercial application of inorganic ferroelectrics is a non-volatile memory for data storage as summarized in the seminal work of Scott.[18] Here, we aim for application in organic non-volatile memories. We show a ferroelectric field-effect transistor and even a dual gate ferroelectric transistor based on δ-PVDF, which behave

as non-volatile memories. They can be programmed at voltages exceeding the coercive field and read-out nondestructively at lower biases.

Field-effect transistors were prepared on heavily doped Si wafers acting as common bottom gate, with thermally grown SiO_2 as bottom gate dielectric and lithographically pre-patterned gold electrodes on a 2 nm Ti adhesion layer. The resulting finger transistors have a channel length of 10000 μm, width between 2 μm and 20 μm and a bottom gate capacitance of 17 nF/cm^2. To reduce gate bias stress, the gate dielectric was passivated with vapor deposited hexamethyldisilazane (HMDS). As semiconductor, a 30 nm thick amorphous gallium–indium–zinc oxide (a-GIZO) was deposited using RF-sputtering. GIZO was deposited from a target with 2:2:1 atomic ratio for Ga:In:Zn.[19] Partial pressure of oxygen inside the sputtering chamber was kept low , < 3%, in order to achieve TFTs operating at low processing temperatures. After GIZO deposition, a short anneal step of 15 min at 150 °C in air was performed. Subsequently, as a second gate dielectric, a 300 nm thick PVDF film was spin-coated at 100°C on top of the a-GIZO films. The dual-gate transistor was finished by evaporating an Au top gate electrode through a shadow mask. Current transport was measured with a Keithley 4200–SCS Semiconductor Characterization System.

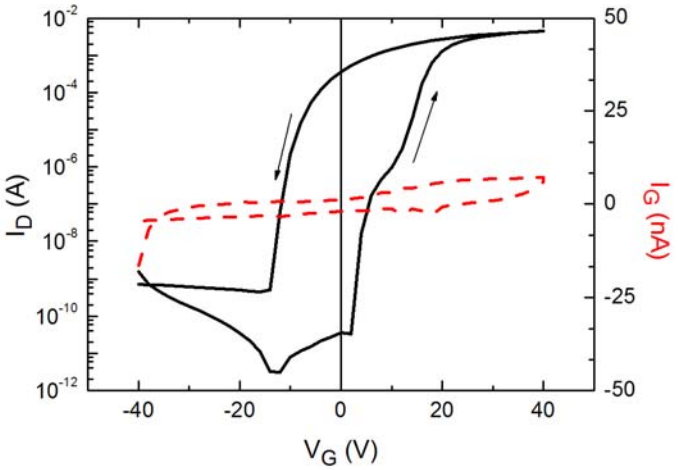

Fig. S5. Single channel ferroelectric field-effect transistor*. Linear transfer curve of a unipolar a-GIZO/δ-PVDF ferroelectric field-effect transistor. Channel length and width are 20 μm and 10000 μm. The drain bias was + 1 V.*

Transfer characteristics were measured in a high-vacuum (10^{-6} mbar) probe station. The device fabrication has not yet been fully optimized. The mobility amounted to about 1 cm^2/Vs.

The chosen device layout allows measuring both a single-gate ferroelectric transistor and a dual-gate ferroelectric transistor. To measure the single-gate a-GIZO/δ-PVDF field-effect transistor the bottom gate was kept floating. The PVDF was electro-formed into the ferroelectric δ-phase by applying a high bias pulse of 100 V for a

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second on the top gate electrode, while grounding the source and drain electrodes. The linear transfer curves are presented in Fig. S5. The transistor switches between a depolarized off-state at negative gate bias and a polarized on-state at positive gate bias.[20] The switching occurs at about +/- 20 V corresponding to the coercive field of δ-PVDF. The switching can be detected in the gate current, but it is masked by parasitic leakage currents. The remanent source-drain current is modulated over 8 orders of magnitude.

A dual-gate ferroelectric field-effect transistor is realized by biasing both the top and bottom gate electrode. The linear transfer curves using a drain bias of +1 V are presented in Fig. S6. The top gate bias is swept. In Fig. S6a the bottom gate is fixed at a positive gate bias and in Fig. S6b the bottom gate is fixed at a negative gate bias. The device physics is complicated. Amorphous GIZO with Au contacts behaves as a unipolar *n*-type semiconductor. The dual-gate transistor contains a bottom and a top channel. When the bottom gate is positive, electrons are accumulated in the bottom channel. Both channels carry current. With a negative bottom gate bias, the bottom channel is depleted of electrons and only the top channel contributes. The current-voltage characteristics then depend on *e.g.* the coupling between the linear bottom capacitance and the ferroelectric top capacitance. A detailed investigation is beyond the scope of this paper. The measurements are included to demonstrate the feasibility of fabricating a ferroelectric dual-gate transistor based on δ-PVDF.

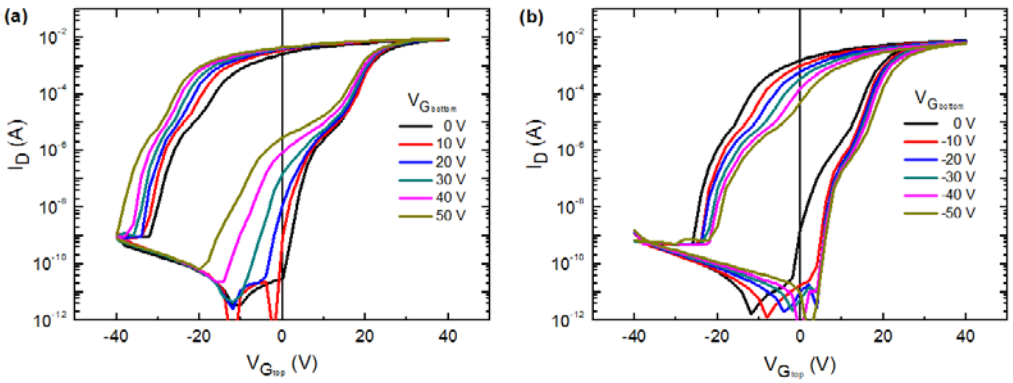

Fig. S6. Dual-gate ferroelectric field-effect transistor. *Linear transfer curves of a dual gate ferroelectric field-effect transistor. The bottom gate dielectric is SiO_2 and the top gate dielectric is δ-PVDF. Channel length and width are 20 μm and 10000 μm. The drain bias was + 1 V. The top gate bias is swept. (a) the bottom gate is fixed at positive gate bias and (b) the bottom gate is fixed at a negative gate bias.*

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